REMARKS

Claims 1-36 are pending. In the Office Action dated June 21, 2007, claims 1-36 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,587,912 to Leddige et al. ("Leddige").

Applicants would like to thank the Examiner for reviewing the Applicants' email correspondence regarding Applicants' reasoning for requesting a telephone interview.

The embodiments disclosed in the present application will now be discussed in comparison to the cited references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the cited references, does not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

The present application is directed toward solving a problem caused by high transfer rates within a memory system. In particular, as transfer rates increase, there is a shorter duration of time in which all the data is in the memory hub prior to transferring the data to the memory controller. This is due to the fact that not all of the data arrives at the memory hub at the exact same time. If the controller begins pulling the data from the memory hub before all of the data has arrived, it will miss some of the data.

In one embodiment, the present application solves this problem by comparing the time in which all of the read data is captured by the memory hub 200 and the time in which all of the read data is pulled from the memory hub 200 to the memory controller 128. In particular, within a read synchronization module 300, a write pointer 312 is incremented at the time when all of the read data is clocked into buffer 308 by a read strobe signal, and a read pointer 314 is incremented when the read data is clocked out of the buffer 308 by a core clock signal. The read pointer 314 and write pointer 312 are compared in a comparator 316 to make sure that there is enough time to capture the data. In addition, the comparator 316 may compare whether there is too much time and is unnecessarily slowing down the process. If appropriate, adjustments are made.

Leddige does not look at the time in which the data goes into or out of the memory hub. Rather, Leddige solves this problem by synchronizing the core clock 724 and an

internal clock signal of the memory hub that is provided to the clock generator 710 via a delay locked loop 758. As known, the delay lock loop 758 compares the phase of the internal clock with the core clock 724. If the clocks are out of phase, the delay lock loop 758 adjusts a delay until the internal clock is in phase with the core clock. The Leddige reference does not look at the *time* when data is clocked into or out of the memory hub. (Emphasis Added). Additionally, the Leddige reference does not look at the relative time of a strobe signal for clocking data into the memory hub and a clock signal used to clock the data out of the memory hub. Therefore the Leddige reference does not disclose or fairly suggest comparing the timing of the clock signals or comparing the timing of a strobe signal and a clock signal, and generating an adjust signal corresponding to the compared timing.

Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out. Independent claim 1 recites, in part, "a read synchronization module...operable to compare timing between coupling read data from the memory devices and coupling read data from the memory hub and to generate an adjust signal corresponding to the compared timing." Leddige does not disclose or fairly suggest this limitation. Rather, Leddige discloses synchronizing a core clock with an internal clock of the memory hub. Therefore, claim 1 is allowable over Leddige.

Independent claim 13 is directed to the memory hub that is included in the memory module of claim 1 and is, therefore, allowable over Leddige for at least the same reasons that claim 1 is allowable.

The memory module of claim 1 is claimed in the context of a computer system in independent claim 20, and is therefore allowable for at least the same reasons that claim 1 is allowable.

Independent claim 8 recites, in part, "a read synchronization module...operable to compare timing between the read data strobe signals and a core clock signal and to generate an adjust signal corresponding to the compared timing." As stated above, Leddige discloses synchronizing a core clock with an internal clock of the memory hub. Therefore, claim 8 is allowable over Leddige.

Independent claim 27 is directed to a method of reading data form a memory module and recites, in part, "comparing timing between receiving the read data and outputting

the read from the memory module and adjusting the timing at which read memory requests are coupled to the memory device interface as a function of the compared timing." Again, Leddige does not disclose or fairly suggest this limitation. Leddige discloses synchronizing a core clock with an internal clock of the memory hub. Therefore, claim 27 is allowable over Leddige.

Independent claim 33 is directed toward a method of coupling read data from a memory device to a buffer and outputting read data from the buffer and recites, in part, "comparing timing between storing the read data in the buffer and outputting the read from the buffer and adjusting the timing at which read memory requests are coupled to the memory device interface as a function of the compared timing." Similar to the statement above, Leddige does not disclose or fairly suggest the above limitation. Leddige discloses synchronizing a core clock with an internal clock of the memory hub. Therefore, claim 33 is allowable over Leddige.

Claims depending from the above independent claims are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims.

All of the claims in the application are clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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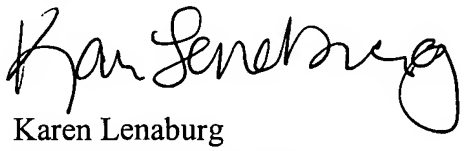

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Enclosures:
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